composite of several 16-word sequences.

Blanking

Some 23 variables are involved in determining whether or not to blank the CRT beam, making this the most complex function in the display circuit.

In addition to those blanking signals already mentioned, a blanking signal is generated for unused columns to the left of the most significant digit. This signal is generated by a comparator. Whenever the output of the D-to-A converter connected to the horizontal counter exceeds a voltage set by the COLUMN BLANKING control, the comparator blanks the beam.

When channel B is displaying data stored in the auxiliary memory, column blanking in both channels is controlled simultaneously. Blanking for the partial display mode is achieved by comparing the count in the vertical counter to the count in the data acquisition section's data index counter. The beam is blanked whenever the vertical count exceeds the data index count because data in memory from that point on is "old" data not wanted on the display.

When the instrument is not in the partial display mode (qualified clock rate >50 Hz), the channel A display is blanked until 16 words are in memory and the trigger word is detected.

There are some differences in the blanking of channels A and B. When channel B displays data from a 1607A, column blanking, partial-display blanking, and so on for channel B are controlled by the 1607A, except in the A&A⊕B mode (channel B displaying differences between 1600A and 1607A data). In this case, channel B column and row blanking is controlled by both the 1600A and 1607A to prevent more bits being displayed than are actually being compared.

Acknowledgments

The 1600S design group was led by Bill Farnbach, who contributed significantly to the instrument design. Product design was by Roger Molnar. Many of the operating concepts were provided by section leader Chuck House and customer requirements were provided by product managers Dick Cochran and Bruce Farly.

References

1. W.A. Farnbach, "The Logic State Analyzer—Displaying Complex Digital Processes in Understandable Form," Hewlett-Packard Journal, January 1974.

Charles T. Small

Chuck Small joined HP in 1966 as a production test technician. Two years later, he transferred to the pulse generator design group, building and debugging prototypes, and in 1972 he moved to the logic state analyzer group where he contributed to the design of Model 1601A. He then undertook the design of the data acquisition portion of Model 1600A. Chuck has an AE degree from the Portland (Oregon) Community College and is doing further academic work at the University of Colorado. Chuck does some woodworking, argues hi-fi matters with colleagues, and is a model railroader (HO gauge). He and his wife have one daughter, 3.

Justin S. Morill, Jr.

Justin Morrill joined Hewlett-Packard in 1972 after getting his Master of Electrical Engineering degree at Rice University (Houston, Texas) where he had also obtained a Bachelor of Arts in Science and Engineering. Before becoming involved in the Logic State Analyzers, he worked on applications of storage CRT's. In his spare time, Justin enjoys the customary Rocky Mountain hiking and backpacking, sometimes packing his 1-year-old son, and he also photographs old mining towns, getting there in his four-wheel-drive vehicle. Justin is also a woodworker.

SPECIFICATIONS

Models 1600A and 1607A Logic State Analyzers

Clock and Data Inputs

REPETITION RATE: 0 to 20 MHz
INPUT RC: 40 kΩ shunted by <14 pF
INPUT BIAS CURRENT: <30 μA
INPUT THRESHOLD: TTL, fixed at approx +1.5V; variable, ±10 Vdc
MAXIMUM INPUT:
LEVEL: −15 to +15 Vdc
SWING: 15 V peak from threshold
MINIMUM INPUT:
SWING: 0.5 V +5% of p-p threshold voltage
CLOCK PULSE WIDTH: 20 ns at threshold
DATA PULSE WIDTH: 25 ns at threshold
DATA SETUP TIME: time data must be present prior to clock transition; 20 ns
HOLD TIME: time data must be present after clock transition; 0 ns

Pattern and Delayed Trigger Outputs

HIGH: >2 V into 50Ω (line driver interface)
LOW: <0.4 V into 50Ω (line driver interface)
PULSE DURATION:
DELAYED TRIGGER: approx 25 ns (RZ format) at 1 V level
PATTERN TRIGGER: approx 25 ns in RZ format at 1 V level with delay set to zero or off. With delay on and not set to zero, pattern trigger output starts on receipt of a pattern trigger signal and ends when the delay ends.

Trigger Arm Input

IMPEDANCE: 50Ω
LEVEL: low state, 0 V to <0.4 V; high state, 2 V to +5 V
PULSE WIDTH: 15 ns minimum at 1.5 V level
ARMING CONDITIONS: If arming pulse positive edge occurs <45 ns after a clock, triggering occurs on same clock cycle. If arming pulse positive edge occurs >75 ns after a clock, triggering occurs on next clock cycle.

1607A X, Y, and Z Axes Outputs

X and Y Axes: −0.6 V to −6 V p-p, ±8 V max into >100 kΩ
Z-AXIS: 0 to 10 V p-p into >1 kΩ
DISPLAY INTERFACE REQUIREMENTS: The 1607A interfaces with any oscilloscope or display with the following input parameters.
X AND Y INPUTS: 0.1 to 1 V/div deflection factors; dc coupled input; and >500 kHz bandwidth
Z-AXIS INPUT: dc coupled with positive blanking; full blanking must occur with <10 V input at 10 mA

General

DISPLAY RATE: variable from <200 ms to >5 s (1600A); <50 ms to >5 s (1607A)
POWER: 100, 120, 220, 240 Vac, −10% +5%, 48 to 440 Hz, 120 VA max
DIMENSIONS: 284 mm (W) × 460 mm (D) × 197 mm (1600A); or 121 mm (1607A); (11.2 × 18.1 × 7.8 or 4.8 inches)
WEIGHT:
MODEL 1600A: 12.7 kg (28 lb)
MODEL 1607A: 6.4 kg (14 lb)
ACCESSORIES SUPPLIED: three 10231B data probes and one 10230B clock probe
PRICES IN U.S.A.:
MODEL 1600A Logic State Analyzer, $4000
MODEL 1607A Logic State Analyzer, $2750
MODEL 1600S includes a 1600A and 1607A with Trigger Bus and Data Cables, $6600
MANUFACTURING DIVISION: COLORADO SPRINGS DIVISION
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